

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

1. (currently amended) A semiconductor device comprising a field effect transistor formed on a SOI substrate, the semiconductor device characterized in comprising:

a gate region formed on a semiconductor film of the SOI substrate; source and drain regions each spaced a specified distance from a channel region formed in the semiconductor film below the gate region, each of the source and drain regions being a first conductive type;

a first extension region that extends from the source region to the channel region; and

a second extension region that extends from the drain region to the channel region,

wherein junction depths of the first and second extension regions are 50% or less of junction depths of the source region and the drain region, and the channel region being a second conductive type.

2. (cancelled)

3. (previously presented) A semiconductor device according to claim 1 characterized in operating in a fully depleted operation mode.

4. (previously presented) A semiconductor device according to claim 1 or claim 3, wherein the SOI substrate is a substrate composed of a glass substrate, a quartz substrate or another insulation substrate and a semiconductor film formed thereon.

5-8. (cancelled)

9. (currently amended) A semiconductor device comprising a field effect transistor characterized in operating in fully depleted operation mode formed on an SOI substrate, the semiconductor device characterized in comprising:

a gate region formed on a semiconductor film of the SOI substrate;  
source and drain regions each spaced a specified distance from a channel region formed in the semiconductor film below the gate region;  
a first extension region that extends from the drain region to the channel region; and

a second extension region that extends from the drain region to the channel region,

wherein junction depths of the first and second extension regions are 50% or less of the junction depth of each of the source region and the drain region, and a thickness of the semiconductor film is 50 nm or less.